

**MANUFACTURE OF MULTI-LAYER WIRING SUBSTRATE**

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**International Class (IPC Edition 6):**

- H05K-003/46
- H05K-003/08
- H05K-003/18
- H05K-003/24
- H05K-003/28
- H05K-003/42
- C23C-018/36
- C23C-022/24
- C23C-028/00
- C25D-003/06
- C25D-003/12
- C25D-003/12

**JAPIO Class:**

- 42.1 (ELECTRONICS-- Electronic Components)
- 12.6 (METALS--- Surface Treatment)

**JAPIO Keywords:**

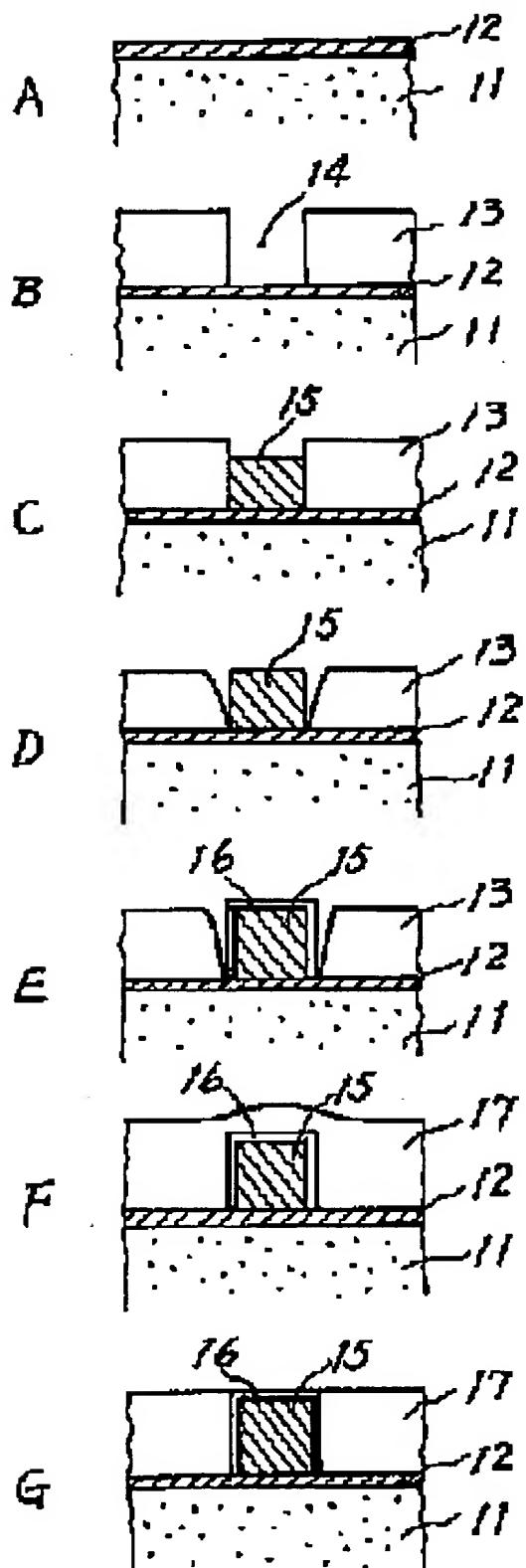
- R004 (PLASMA)
- R044 (CHEMISTRY--- Photosensitive Resins)
- R124 (CHEMISTRY--- Epoxy Resins)
- R129 (ELECTRONIC MATERIALS--- Super High Density Integrated Circuits, LSI & GS

**Abstract:**

PURPOSE: To eliminate factors causing deterioration of a bonding between copper and polyimide by forming selectively a protective film on a via stud or wiring or both subjected to patterning.

CONSTITUTION: A laminate film 12 to serve as an undercoat for a load dispatching layer when electroplating a substrate 11 is formed by continuous vacuum evaporation. Further, a dielectric film 13 which will become an organic resin is made. Next, the dielectric film is patterned with minute holes and grooves. This is followed by electrolytic copper plating to fill a via hole 14. After ashing O<sub>2</sub>(sub 2), because of a fast plasma etching rate of a resist in the vicinity of a via stud, a via surface part is exposed. Next, after a series of treatment prior to plating are performed, electroless chrome plating is performed to form a protective film 16. Also, as the protective film 16, electroless or electrolytic cobalt plating is effective. Next, after the resist is peeled, an organic resin film 17 is applied and polishing is conducted to provide a heading of the via stud. This enables the via stud and an insulating layer to be in good adhesion.

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JAPIO

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